14-20 are respectfully requested to remove multiple dependent claims, reference symbols, and to place the claims in accepted U.S. format.

IN THE CLAIMS

Please amend replacement claims 1-13, as follows (a marked-up copy of the claims is attached to this document):

1. (Amended-Clean Text) A circuit arrangement for electrically generating a ringing impedance in telephone terminals by means of at least one transistor and a capacitor, the ringing impedance being adaptable by controlling the resistance of the transistor, having a ringing alternating voltage which can be tapped between a first input terminal and a second input terminal, wherein a digital controller is provided for setting the ringing impedance, said controller adapting the ringing impedance to the given conditions by generating from the ringing alternating voltage a control voltage for controlling the transistor,

the digital controller has a programmable digital filter, and

the transmission function of the digital filter can be set by programing the associated filter coefficients.

2. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein the digital filter is a component of a programmable digital signal processor or microprocessor.

3. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein a digital power inverter circuit is connected upstream of the digital filter and a digital rectifier circuit is connected downstream of the digital filter.

4. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, comprising:

- a rectifier circuit for rectifying the ringing alternating voltage,
- a capacitor which is connected between an input terminal and rectifier circuit,
- a transistor which is arranged by means of its load path between the outputs of the rectifier circuit,
- a first and second voltage, which are rectified from the ringing alternating voltage by means of the rectifier circuit, being fed to the controller, and
- the controller making available a control voltage for driving the transistor.

5. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein the controller has an analog integrator circuit which is connected upstream of the transistor and which makes available an output signal which is integrated from the difference between a first input voltage and a second input voltage and which drives the transistor.

6. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein a voltage divider is provided which makes available a component voltage from the voltage which is present at the one output of the rectifier circuit.

7. (Amended-Clean Text) The circuit arrangement as claimed in claim 3, wherein the digital power inverter circuit , the digital filter and the digital rectifier circuit are together integrated on a semiconductor chip of digital design.

8. (Amended-Clean Text) The circuit arrangement as claimed in claim 3, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

9. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein

- a first capacitor, the load path of a first transistor and a first resistor are arranged in series between the first terminal and a reference potential,
- a second capacitor, the load path of a second transistor and a second resistor are arranged in series between the second terminal and the reference potential,
- a first and a second input potential of the ringing alternating voltage being fed to the controller and
- the controller making available a first control voltage for driving the first transistor and a second control voltage for driving the second transistor.

10. (Amended-Clean Text) The circuit arrangement as claimed in claim 9, wherein the controller

- has a first analog integrator circuit which is connected upstream of the first transistor and which makes available an output signal which is integrated from the difference between a first input voltage and a second input voltage and which drives the first transistor, and
- has a second analog integrator circuit which is connected upstream of the second transistor and which makes available an output signal which is integrated from the difference between a third input voltage and a fourth input voltage and which drives the second transistor.

11. (Amended-Clean Text) The circuit arrangement as claimed in claim 9, wherein a first voltage divider is provided which makes available a first component voltage from the first potential of the ringing alternating voltage, and

a second voltage divider is provided which makes available a second component voltage from the second potential of the ringing alternating voltage.

12. (Amended-Clean Text) The circuit arrangement as claimed in claim 10, wherein at least one analog/digital converter, which is connected upstream of the digital filter, is provided, and at least one digital/analog converter, which is connected downstream of the digital rectifier circuit, is provided, the analog/digital converters, the digital/analog

converters and the analog integrator circuits being together integrated on a semiconductor chip of analog design.

13. (Amended-Clean Text) The circuit arrangement as claimed claim 4, wherein at least one of the transistors is embodied as an n-channel-MOSFET.

Please add new claims 14-20 as follows:

---14. The circuit arrangement as claimed in claim 2, wherein a digital power inverter circuit is connected upstream of the digital filter and a digital rectifier circuit is connected downstream of the digital filter.

15. The circuit arrangement as claimed in claim 4, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

16. The circuit arrangement as claimed in claim 5, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

17. The circuit arrangement as claimed in claim 6, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

18. The circuit arrangement as claimed in claim 7, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

19. The circuit arrangement as claimed in claim 2, wherein

- a first capacitor, the load path of a first transistor and a first resistor are arranged in series between the first terminal and a reference potential,
- a second capacitor, the load path of a second transistor and a second resistor are arranged in series between the second terminal and the reference potential,
- a first and a second input potential of the ringing alternating voltage being fed to the controller and
- the controller making available a first control voltage for driving the first transistor and a second control voltage for driving the second transistor.